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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,756	07/24/2003	Kevin Traynor	032674-200	1739

7590 10/01/2007

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
10/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/626,756	TRAYNOR ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Application Status

Applicants' RCE filed 7/30/2007 to continue prosecution of this application is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Specifically, the phrase "prioritizes the servicing of interrupt requests" (emphasis added) does not have adequate support from the originally filed specification. It is noted that Applicants have cited paragraph [0004] for support. However, as disclosed by the originally filed specification, paragraph [0004] is a portion of the "Background [of Invention]" describing the typical prior art, and therefore, cannot be a part of Applicants' claimed invention. The only portion of the specification describing the use of "priority" according to Applicants' claimed invention is paragraph [0030], which is reproduced below for ease of reference and convenience.

[0030] The added flexibility afforded through mapping provides many advantages over conventional interrupt-sharing arrangements. Consider, for example, where the IC 340 has assigned priorities to each of the interrupt inputs INT-01 through INT-N. The priority of an interrupt source 310 can be changed dynamically (and repeatedly) by setting the associated control bits to enable requests to be mapped only to the interrupt input having the desired priority level. Moreover, the set of enabled interrupt sources 310 can be changed dynamically according to user preferences, system state, system demands, or a host of other conditions.

If Applicants disagree with the Examiner, Applicants are required to point to the specification by citing page and line number, and to the drawings, for support of the phrase "prioritizes the servicing of interrupt requests" (emphasis added).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Wach (5,530,875).

With regard to claim 1, Wach discloses a method for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, which generates interrupt requests, comprising the steps of: mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs of an interrupt controller that receives the interrupt requests and prioritizes the servicing of the received requests; and selectively enabling interrupt requests from each of the plurality of interrupt sources to be received at one or more of the plurality of interrupt inputs (Wach discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

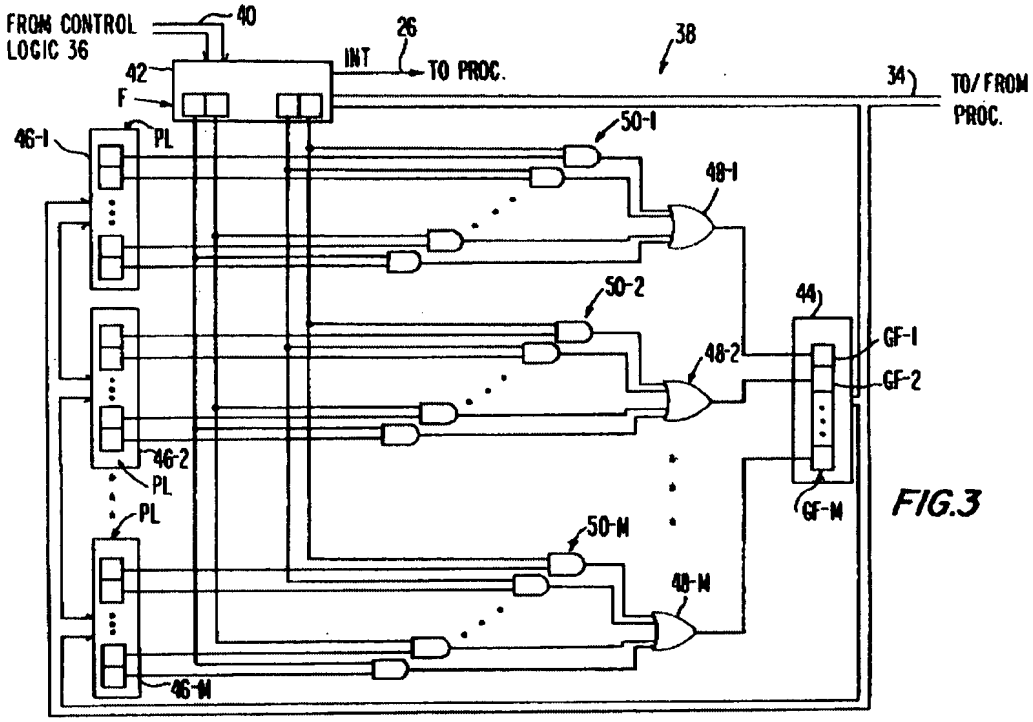

FIG.3

At the outset, in order to have a clear understanding of the following discussion, it is important to note that the interrupt requests can be generated from register 44 instead of register 42 (see column 11, lines 10-15). In addition, the term "group" used in Wash includes group that has only one interrupt resource (see column 11, lines 47-49).

As shown above and specifically described in column 4, line 63 to column 6, line 43; column 10, line 55 to column 11, line 48, the number of storage locations F in register 42 is equal to the number of interrupt sources, any one of which may cause the transmission of the interrupt signal to processor 14. Also, the locations F correspond one-to-one to the interrupt sources. The plurality of interrupt sources are routed or mapped to a plurality of interrupt inputs represented by a plurality of storage locations GF of the group register 44 (defining the so-called "interrupt controller") of the interrupt manager 38; wherein the interrupt requests are enabled when any one or more of the storage locations GF of the interrupt controller 44 are enabled or set. Thus, it is clear that in Wash, as shown in Fig. 3 above, when the interrupt requests from interrupt sources are received at (mapped to) the interrupt inputs GF of the interrupt controller 44. Further, in Wash, at least one of the interrupt sources is assigned priorities by connecting one of the storage locations F (representing interrupt sources) with one of the storage locations GF (interrupt inputs) of the interrupt controller 44. See at least column 2, lines 41-51, and claim 2. Thus, it is clear that such a one-to-one connection between each of the interrupt sources (representing by locations F) and each of the interrupt inputs GF of the interrupt controller 44 is prioritized. In other words, the

interrupt inputs GF are selectively enabled (prioritized) by the interrupt controller 44 to assign priorities to each one-to-one connection (mapping) between the interrupt sources and the interrupt inputs. Further, in Wash, a masking bit is used to enable or disable interrupt requests from each of a plurality of interrupt sources to one or more of the plurality of interrupt inputs. Specifically, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

With regard to claim 2, as discussed above, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

With regard to claim 3, as discussed above, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked. Further, as also discussed above, each location PL corresponds to each of interrupt source. Thus, it is clear that a control bit value can be selectively set in each of location PL corresponding to the mapped interrupt source/interrupt input combination.

With regard to claim 4, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be set according to user preferences.

With regard to claim 5, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be dynamically modified according to user preferences.

With regard to claim 6, it is clear that the control bit values must be defined according to system requirements. Further, it is also clear that the system of Wash comprises the processor, at least one interrupt source, and at least one interrupt input.

With regard to claims 7-12, see discussion above, since the subject matter presented in claims 7-12 has already been addressed.

With regard to claim 13, as clearly shown in the figure above, the logic that selectively enables comprises, for each mapped interrupt source/interrupt input combination, a logical AND (50) for ANDing each interrupt source with a respective control bit value.

With regard to claim 14, Wash discloses a system for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources (Wach discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

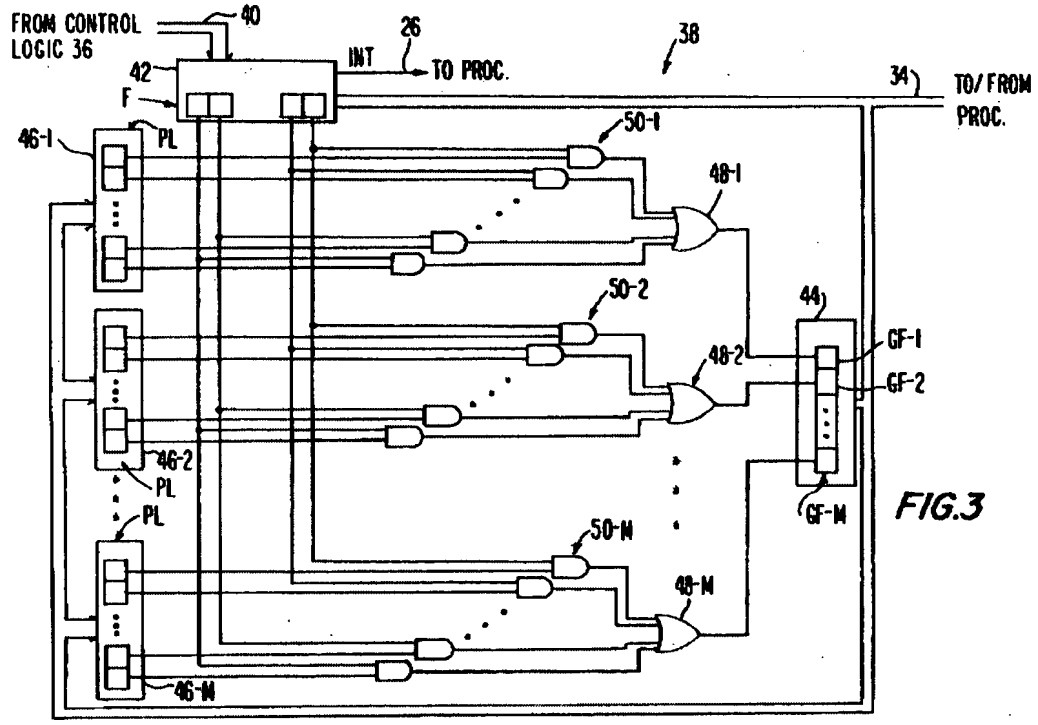

FIG.3

, comprising: for each of said plurality of interrupt inputs: a plurality of logical ANDs, each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor (a plurality of AND gates 50, each having an input to receive an interrupt request signal from an interrupt source to interrupt the processor; see also discussion above regarding claim 1); a plurality of control bits each corresponding to an interrupt source and each respectively providing a control bit value to the corresponding logical AND (a plurality of masking bits, each can be set in the location PL to provide a control value to the other input of AND gate 50; see also discussion regarding claim 1 above), wherein, based on the control bit value, a corresponding interrupt request signal is

provided at an output of the corresponding logical AND (based on the control bit value provided at one input of the AND gate, an interrupt request signal is provided at output of the AND gate 50; see also discussion above regarding claim 1); a logical OR arranged to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs (as clearly discussed above regarding claim 1, the OR gate 48 is arranged to indicate the presence of a corresponding interrupt request signal from at least one output of the plurality of AND gates 50 to the interrupt input; see also discussion above regarding claim 1).

With regard to claims 15-20, see discussion above, since the subject matter presented in claims 15-20 has already been addressed.

Response to Arguments

Applicants' arguments filed 7/30/2007 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification

cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112, 2nd Paragraph Rejection:

Applicants' amendments overcome the 35 USC 112, 2nd paragraph Rejection.

The Armstrong 102 Rejection:

The Armstrong 102 Rejection is withdrawn in view of Applicants' amendments to the claims, NOT because of Applicants' arguments.

The Wach 102 Rejection:

With regard to claims 1-23, Applicants argued that "[t]he operation of the system described in the Wach patent is different from the operation of the claimed method and apparatus. In the Wach patent, the register 44 must be read by the processor 14 in order for the interrupt source to be identified (column 6, lines 21-24 of the Wach patent). This is one of the drawbacks of the prior art identified in Applicants' specification (see paragraph [0006] of Applicants' specification). It is a drawback because the interrupt manager 38 and processor 14 must determine which interrupt

source is issuing the interrupt request by polling the interrupt group in register 44. The Wach patent merely reduces the number of times the processor polls the register as described at column 6, lines 25-35."

In response to Applicants' argument, at the outset, it is noted that Applicants, instead of pointing out the supposed errors in the Examiner's rejection by specifically point out the claim language that is not disclosed by Wach, incorrectly interpret the Wach reference. It is also noted that portions of the Wach reference (cited above by Applicants) are taken out of context. With regard to "polling," contrary to Applicants' argument, the is nothing in Wach that even remotely suggests the use of "polling" as alleged by Applicants.

As clearly pointed out in the rejection, which is reproduced below (with emphasis added):

Wach discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

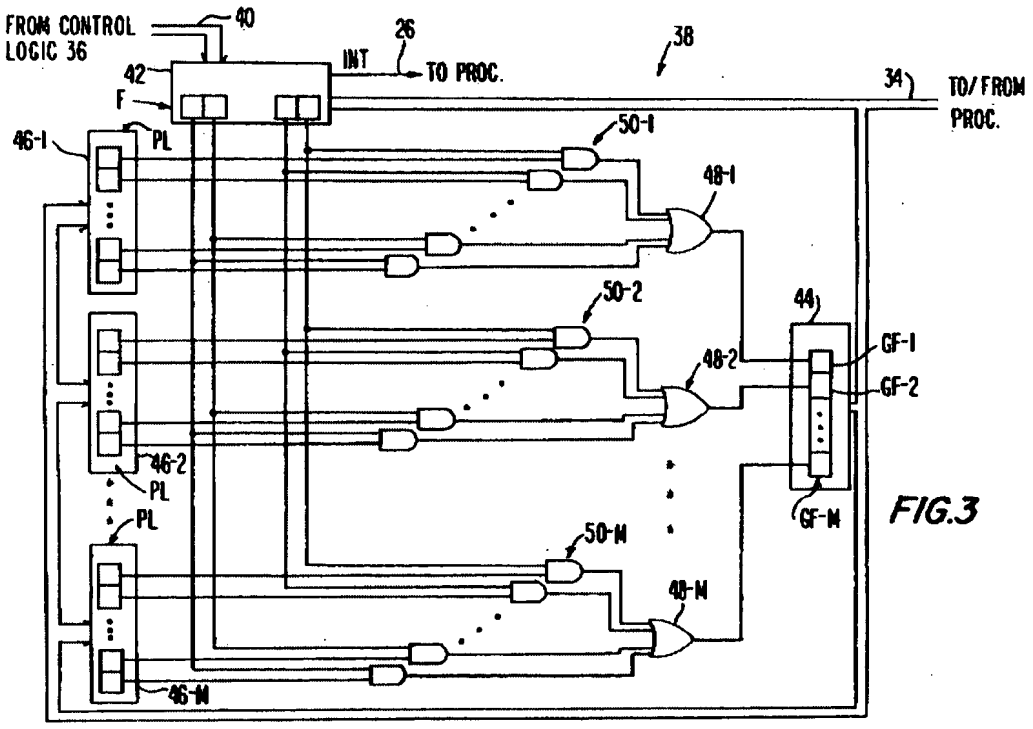

FIG.3

At the outset, **in order to have a clear understanding of the following discussion, it is important to note that the interrupt requests can be generated from register 44 instead of register 42 (see column 11, lines 10-15). In addition, the term "group" used in Wash includes group that has only one interrupt resource (see column 11, lines 47-49).**

As shown above and specifically described in column 4, line 63 to column 6, line 43; column 10, line 55 to column 11, line 48, the number of storage locations F in register 42 is equal to the number of interrupt sources, any one of which may cause the transmission of the interrupt signal to processor 14. Also, the locations F correspond one-to-one to the interrupt sources. The plurality of interrupt sources are routed or

mapped to a plurality of interrupt inputs represented by a plurality of storage locations GF of the group register 44 (defining the so-called "interrupt controller") of the interrupt manager 38; wherein the interrupt requests are enabled when any one or more of the storage locations GF of the interrupt controller 44 are enabled or set. In other words, in Wash, as shown in Fig. 3 above, the interrupt requests from interrupt sources are received at (mapped to) the interrupt inputs GF of the interrupt controller 44. Further, in Wash, at least one of the interrupt sources is assigned priorities by connecting one of the storage locations F (representing interrupt sources) with one of the storage locations GF (interrupt inputs) of the interrupt controller 44. See at least column 2, lines 41-51, and claim 2. Thus, it is clear that such a one-to-one connection between each of the interrupt sources (representing by locations F) and each of the interrupt inputs GF of the interrupt controller 44 is prioritized. In other words, the interrupt inputs GF are selectively enabled (prioritized) by the interrupt controller 44 to assign priorities to each one-to-one connection (mapping) between the interrupt sources and the interrupt inputs. Further, in Wash, a masking bit is used to enable or disable interrupt requests from each of a plurality of interrupt sources to one or more of the plurality of interrupt inputs. Specifically, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

Applicants further argued that "[t]he group register 44 of the Wach patent does not constitute an interrupt controller, as that term is employed in the context of the

present invention and commonly understood by those of ordinary skill in the art. Rather, as explained above, it is a passive storage device that must be interrogated by the interrupt controller in the processor to determine the origin of an interrupt received on line 26."

Contrary to Applicants' argument, it is clear that a plurality of location GF of register 44 is readable as a plurality of interrupt inputs. As disclosed in [0012], page 4 of Applicants' originally filed specification and as shown in Fig. 3, the interrupt inputs are defined as follows:

> **[0012]** In yet another aspect of the invention, a system is disclosed for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources. The system comprises, for each interrupt input, a plurality of logical ANDs, each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor. A plurality of control bits each correspond to an interrupt source and each respectively provide a control bit value to the corresponding logical AND, wherein, based on the control bit value, a corresponding interrupt request signal is provided at an output of the corresponding logical AND. A logical OR is arranged to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs.

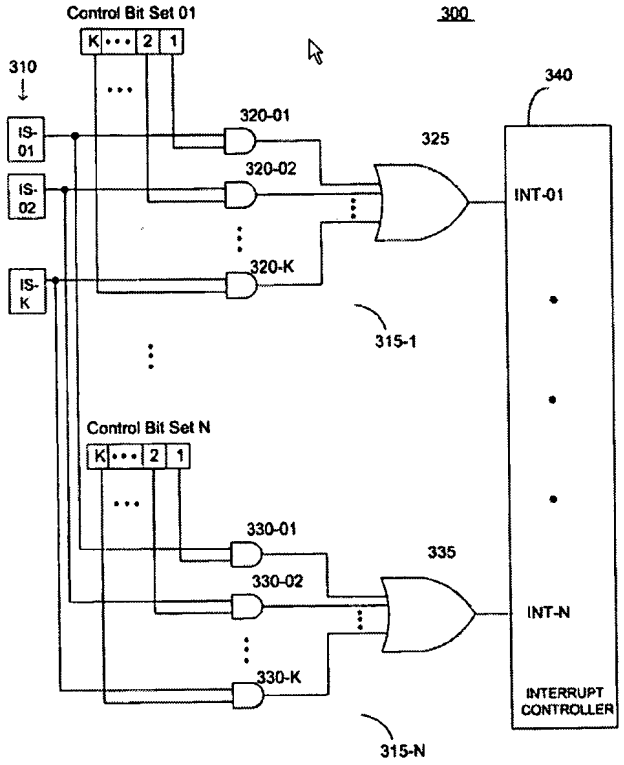

FIG. 3

Identically disclosed and shown in **Fig. 3 of Wach:**

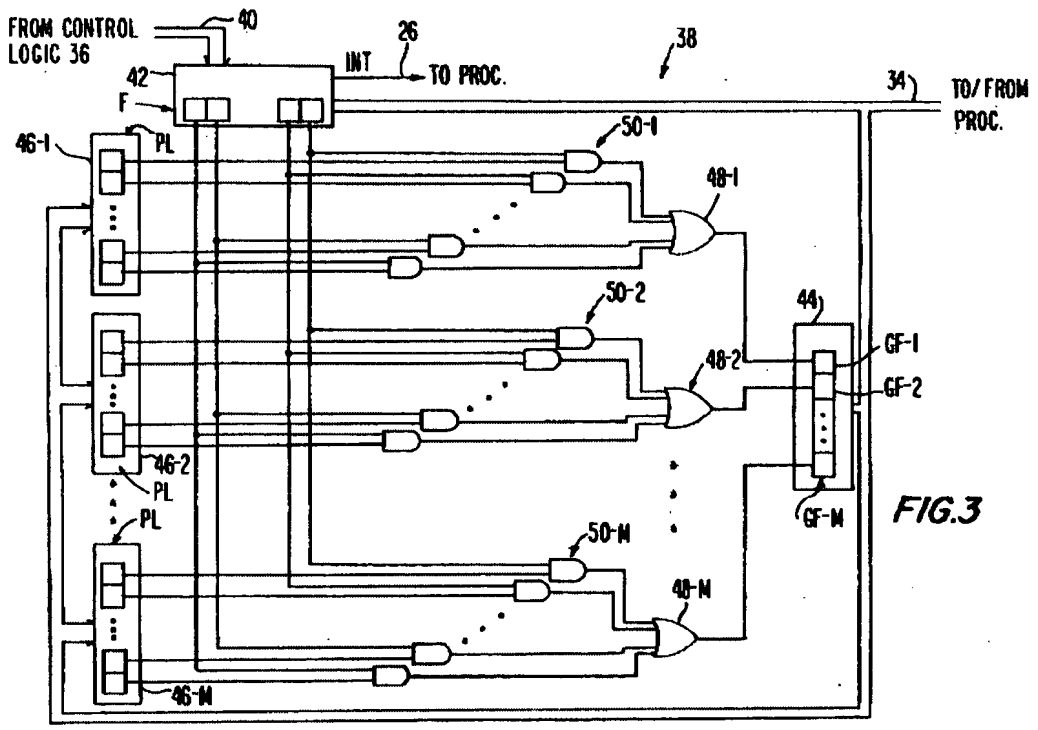

FIG.3

It is clear from at least Fig. 3 of Wach, a logical OR is arranged to indicate, to the locations GF or interrupt inputs of the interrupt controller 44 of the interrupt manager 38, the presence of a corresponding interrupt request signal from at least one output of a plurality of logical AND gates.

Applicants also argued that "[t]o clarify the distinction between these elements, claim 1 now specifies that the interrupt controller, which has a plurality of interrupt inputs, receives interrupt requests and prioritizes the servicing of received requests. See, for example, the specification at paragraph [0004]. It is respectfully submitted that the group register 44 of the Wach patent does not meet this definition of an interrupt controller."

In response to Applicants' argument, at the outset, it is noted that the phrase "prioritizes the servicing of interrupt requests" (emphasis added) does not have adequate support from the originally filed specification. It is noted that Applicants have cited paragraph [0004] for support. However, as disclosed by the originally filed specification, paragraph [0004] is a portion of the "Background [of Invention]" describing the typical prior art, and therefore, cannot be a part of Applicants' claimed invention. The only portion of the specification describing the use of "priority" according to Applicants' claimed invention is paragraph [0030], which is reproduced below for ease of reference and convenience.

> **[0030] The added flexibility afforded through mapping provides many advantages over conventional interrupt-sharing arrangements. Consider, for example, where the IC 340 has assigned priorities to each of the interrupt inputs INT-01 through INT-N. The priority of an interrupt source 310 can be changed dynamically (and repeatedly) by setting the associated control bits to enable requests to be mapped only to the interrupt input having the desired priority level. Moreover, the set of enabled interrupt sources 310 can be changed dynamically according to user preferences, system state, system demands, or a host of other conditions.**

See the 112 Rejection above.

In any event, contrary to Applicants' argument, in Wash, at least one of the interrupt sources is assigned priorities by connecting one of the storage locations F (representing interrupt sources) with one of the storage locations GF (interrupt inputs) of the interrupt controller 44. See at least column 2, lines 41-51, and claim 2. Thus, it is clear that such a one-to-one connection between each of the interrupt sources

(representing by locations F) and each of the interrupt inputs GF of the interrupt controller 44 is prioritized. In other words, the interrupt inputs GF are selectively enabled (prioritized) by the interrupt controller 44 to assign priorities to each one-to-one connection (mapping) between the interrupt sources and the interrupt inputs. Based on priority, interrupts to the processor will be serviced by invoking appropriated interrupt routines.

With regard to claim 14, Applicants argued that "[i]ndependent claim 14 recites, in combination with other features, a logical OR arranged to indicate, to the interrupt inputs of an interrupt controller that receives the interrupt requests, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs. As argued above, the Wach patent does not disclose interrupt inputs of an interrupt controller that receives the interrupt requests (emphasis in the original) on which are indicated the presence of a corresponding interrupt request signal as recited in independent claim 14."

Contrary to Applicants' argument, it is clear from at least Fig. 3 of Wach, a logical OR is arranged to indicate, to the locations GF or interrupt inputs of the interrupt controller 44 of the interrupt manager 38, the presence of a corresponding interrupt request signal from at least one output of a plurality of logical AND gates. Further, it is also clear from discussion above that the plurality of interrupt sources are routed or mapped to a plurality of interrupt inputs represented by a plurality of storage locations GF of the group register 44 (defining the so-called "interrupt controller") of the interrupt manager 38; wherein the interrupt requests are enabled when any one or more of the

storage locations GF of the interrupt controller 44 are enabled or set. In other words, in Wash, as shown in Fig. 3 above, the interrupt requests from interrupt sources are received at (mapped to) the interrupt inputs GF of the interrupt controller 44.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner